#5

Please type a plus sign (+) inside this box → +

OIPE JC174 OCT 0 8 2003 PATENT & TRADEMARK OFFICE

PTO/SB/08A (08-00)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 3

Complete if Known	
Application Number	09/749,750
Filing Date	December 28, 2000
First Named Inventor	MAIYURAN et al
Group Art Unit	2186
Examiner Name	S.C. Elmore
Attorney Docket Number	2207/10608

RECEIVED
OCT 10 2003
Technology Center 2100

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	
SE		6,381,671	B1	Ayukawa et al	April 30, 2002	
SE		6,115,793		Gruber	September 5, 2000	
SE		US 2002/012901	A1	Maiyuran et al	Pub. date September 12, 2002	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
SE	a	Agarwal et al, "Column-Associative Caches: A Technique for Reducing the Miss Rate of Direct-Mapped Caches", Proceedings, The 20th Annual Intl Symposium on Computer Architecture, IEEE Computer Society, Technical Committee on Computer Architecture, Association for Computing Machinery SIGARCH, pp 169-190, San Diego, California, May 16-19, 1993	
SE	b	Alexander et al, "Distributed Prefetch-buffer/Cache Design for High Performance Memory Systems", Proceedings, Second Intl Symposium on High-Performance Computer Architecture, IEEE Computer Society, Technical Committee on Computer Architecture, pp 254-263, San Jose, California, February 3-7, 1996	
SE	c	Burger et al, "The SimpleScalar Tool Set, Version 2.0", *Computer Sciences Department Technical Report*, No. 1342, The University of Wisconsin, Madison, Wisconsin, June 1997	
SE	d	Edmondson et al, "Internal Organization of the Alpha 21164, a 300-MHz 64-bit Quad-issue CMOS RISC Microprocessor", *Digital Technical Journal*, Vol. 7, No. 1, pp 119-135, 1995	
SE	e	Hill, Mark D., "A Case for Direct-Mapped Caches", *Computer*, pp 25-40, December 1988	

Examiner Signature	S. Elmore	Date Considered	4-19-04

Please type a plus sign (+) inside this box → +

PTO/SB/08A (08-00)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 2 of 3

Complete if Known	
Application Number	09/749,750
Filing Date	December 28, 2000
First Named Inventor	MAIYURAN et al
Group Art Unit	2186
Examiner Name	S.C. Elmore
Attorney Docket Number	2207/10608

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
SE	1	Juan et al, "The Difference-bit Cache", Proceedings, The 23rd Annual Int'l Symposium on Computer Architecture, ACM SIGARCH, IEEE Computer Society, TCCA, pp 114-120, Philadelphia, Pennsylvania, May 22-24, 1996	
SE	2	Kessler et al, "Inexpensive Implementation of Set-Associativity", Proceedings, The 16th Annual Intl Symposium on Computer Architecture, IEEE Computer Society Press, pp 131-139,1989	
SE	3	Rau et al, "Pseudo-Randomly Interleaved Memory", Proceedings, The 18th Annual Intl Symposium on Computer Architecture, Association for Computing Machinery, pp 74-83, Toronto, Canada, May 27-30, 1991	
SE	4	Rivers et al, "On Effective Data Supply for Multi-Issue Processors", Proceedings, Intl Conference on Computer Design, VLSI in Computers and Processors, IEEE Computer Society Technical Committee on Design Automation, IEEE Circuits and Systems Society, pp 519-528, Austin, Texas, Oct. 12-15, 1997	
SE	5	Sánchez et al, "A Locality Sensitive Multi-Module Cache with Explicit Management", Proceedings of the 1999 Intl Conference on Supercomputing, ICS '99, Rhodes, Greece	
SE	6	Sohi et al, "High-Bandwidth Data Memory Systems for Superscalar Processors", ASPLOS-IV Proceedings, Fourth Intl Conference on Architectural Support for Programming Languages and Operating Systems, pp 53-62, Santa Clara, California, April 8-11, 1991	
SE	7	Wilson et al, "Increasing Cache Port Efficiency for Dynamic Superscalar Microprocessors", Proceedings, The 23rd Annual Intl Symposium on Computer Architecture, ACM SIGARCH, IEEE Computer Society, TCCA, pp 147-157, Philadelphia, Pennsylvania, May 22-24, 1996	
SE		Wilson et al, "Designing High Bandwidth On-Chip Caches", "The 24th Annual Intl Symposium on Computer Architecture, Conference Proceedings, ACM, pp 121-132, Denver, Colorado, June 2-4, 1997	

Examiner Signature	S. Elmore	Date Considered	4-19-04

Please type a plus sign (+) inside this box →

PTO/SB/08A (08-00)
Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 3 of 3

Complete if Known	
Application Number	09/749,750
Filing Date	December 28, 2000
First Named Inventor	MAIYURAN et al
Group Art Unit	2186
Examiner Name	S.C. Elmore
Attorney Docket Number	2207/10608

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
SE	4	Wilton et al, "An Enhanced Access and Cycle Time Model for On-Chip Caches", Digital WRL Research Report 93/5, Palo Alto, California, July 1994	
SE	v	Shanley, T., *Pentium® Pro Processor System Architecture*, Chapter 5, pp.61-118, Addison-Wesley Developers Press, 1997	
SE	l	Rivers et al, "On High-Bandwidth Data Cache Design for Multi-Issue Processors", IEEE, Proceedings, Micro-30, Dec. 1-3, 1997, Research Triangle Park, North Carolina	
SE	l	Neefs et al, "A Technique for High Bandwidth and Deterministic Low Latency Load/Store Accesses to Multiple Cache Banks, 6th Int'l. Symposium on High-Performance Computer Architecture HPCA-6, IEEE, 1999, Los Alamitos, California	
SE	4	Calder et al, "Predictive Sequential Associative Cache", IEEE, Proceedings 2nd Int'l. Symposium on High-Performance Computer Architecture, Feb. 3-7, 1996, San Jose, California	
SE	,	Cho et al, "Decoupling Local Variable Accesses in a Wild-Issue Superscaler Processor, Proceedings of the 26th Annual Int'l. Symposium on Computer Architecture, May 1999	

Examiner Signature	S. Elmore	Date Considered	4-19-04